Claims

1. A clock signal extraction device for extracting a clock
signal from a periodic data signal, comprising:
5   - a phase detector (104, 106) for detecting a first phase
difference between rising edges of said data signal and a
rising edges clock signal and for detecting a second phase
difference between falling edges of said data signal and a
falling edges clock signal; and
10   - a clock generator (110, 112) for generating said rising
edges clock signal so that said first phase difference is
minimized, for generating said falling edges clock signal so
that said second phase difference is minimized, and for
generating said clock signal in dependence on said first
15   phase difference and said second phase difference.

2. The device according to claim 1,
c h a r a c t e r i z e d   i n   t h a t
said clock generator (104, 106) generates said clock signal
20   based on an average of said first phase difference and said
second phase difference.

3. The device according to claim 1 or 2,
c h a r a c t e r i z e d   i n   t h a t
25   said clock generator comprises:
- a first clock generator (110) for generating said rising
edges clock signal;
- a second clock generator (112) for generating said falling
edges clock signal;
30   - a third clock generator (114) for generating said clock
signal; and
- a controller (108) for processing said first phase
difference and said second phase difference and for

controlling said first, second and third clock generator
(110, 112, 114).

4. The device according to claim 1, 2 or 3,
5   c h a r a c t e r i z e d   i n   t h a t
said phase detector comprises:
- a first phase detector (104) for detecting said first phase
difference between said rising edges of said data signal and
said rising edges clock signal; and
10   - a second phase detector (106) for detecting said second
phase difference between said falling edges of said data
signal and said falling edges clock signal.

5. The device according to claim 3 or 4,
15   c h a r a c t e r i z e d   i n   t h a t
each of said first, second and third clock generators (110,
112, 114) comprises a voltage controlled oscillator.

6. The device according to claim 3, 4 or 5,
20   c h a r a c t e r i z e d   i n   t h a t
said controller (108) comprises a phase pump and a loop
filter.

7. The device according to one of the preceding claims,
25   c h a r a c t e r i z e d   i n   t h a t
said device is used in a data extraction device (100) for
extracting data from said data signal according to a rate of
said clock signal.

30   8. The device according to claim 7,
c h a r a c t e r i z e d   i n   t h a t

said controller (108) controls said clock generator (110, 112, 114) for generating said clock signal such that the error rate of the extracted data is minimized.

5   9. The device according to claim 7 or 8,
     c h a r a c t e r i z e d   i n   t h a t
     said data extraction device (100) comprises a data sampler (116) for sampling said data signal.

10   10. The device according to claim 9,
     c h a r a c t e r i z e d   i n   t h a t
     said data sampler (116) comprises a D-type flip-flop.

     11. A method for extracting a clock signal from a periodic
15   data signal, comprising:
     - detecting a first phase difference between rising edges of said data signal and a rising edges clock signal and detecting a second phase difference between falling edges of said data signal and a falling edges clock signal; and
20   - generating said rising edges clock signal so that said first phase difference is minimized, generating said falling edges clock signal so that said second phase difference is minimized, and generating said clock signal in dependence on said first phase difference and said second phase difference.
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     12. The method to claim 11,
     c h a r a c t e r i z e d   i n   t h a t
     said step of generating comprises generating said clock signal based on an average of said first phase difference and
30   said second phase difference.

     13. The method according to claim 11 or 12,
     c h a r a c t e r i z e d   i n   t h a t

said step of generating further comprises:

- processing said first phase difference and said second
phase difference; and

- generating and controlling said rising edges clock signal,

5   said falling edges clock signal, and said clock signal.

14. The method according to claims 11 to 13,
c h a r a c t e r i z e d   i n   t h a t
said method further comprises:

10   - extracting data from said data signal according to a rate
of said clock signal.

15. The method according to claim 14,
c h a r a c t e r i z e d   i n   t h a t

15   said step of generating further comprises generating said
clock signal such that the error rate of said extracted data
is minimized.

16. The device or the method according to one of the

20   preceding claims,
c h a r a c t e r i z e d   i n   t h a t
said data signal is an optical data signal.